ABSTRACT OF THE DISCLOSURE

The semiconductor device comprises a gate electrode 26 formed on a semiconductor substrate 10, a source region 45a having a lightly doped source region 42a and a heavily doped source region 44a, a drain region 45b having a lightly doped drain region 42b and a heavily doped drain region 44b, a first silicide layer 40c formed on the source region, a second silicide layer 40d formed on the drain region, a first conductor plug 54 connected to the first silcide layer and a second conductor plug 54 connected to the second silicide layer. The heavily doped drain region is formed in the region of the lightly doped region except the peripheral region, and the second silicide layer is formed in the region of the heavily doped drain region except the peripheral region. Thus, the concentration of the electric fields on the drain region can be mitigated when voltages are applied to the drain region. Thus, even with the silicide layer formed on the source/drain region, sufficiently high withstand voltages of the high withstand voltage transistor can be ensured. Furthermore, the drain region alone has the above-described structure, whereby the increase of the source-drain electric resistance can be prevented while high withstand voltages can be ensured.